

What is claimed is:

1 1. An interconnect structure, comprising:
2 a substrate;
3 a first metal line disposed on the substrate;
4 a first insulating layer disposed on the substrate,
5 covering the first metal line;
6 a second metal line disposed on the first insulating
7 layer;
8 a second insulating layer covering the second metal
9 line;
10 ITO (indium tin oxide) wiring electrically
11 connecting the first and second metal lines;
12 and
13 a passivation structure disposed on the second
14 insulating layer with an opening therein to
15 expose and enclose the ITO wiring.

1 2. The interconnect structure as claimed in claim
2 1, wherein the substrate is a TFT-array substrate for a
3 flat display panel.

1 3. The interconnect structure as claimed in claim
2 1, wherein the first and second metal lines, the ITO
3 wiring and the passivation structure are disposed in a
4 non-display area of the TFT-array substrate.

1 4. The interconnect structure as claimed in claim
2 3, wherein the first metal line is a gate metal line
3 formed simultaneously with gate metal lines in a display
4 area of the TFT-array substrate.

1 5. The interconnect structure as claimed in claim
2 3, wherein the second metal line is a source/drain metal
3 line that is formed simultaneously with source/drain
4 metal lines on a display area of the TFT-array substrate.

1 6. The interconnect structure as claimed in claim
2 1, wherein the ITO wiring comprises a first ITO electrode
3 disposed in the first and second insulating layers in
4 contact with the first metal line, a second ITO electrode
5 disposed in the second insulating layer in contact with
6 the second metal line, and an ITO layer connecting the
7 first and second ITO electrodes.

1 7. The interconnect structure as claimed in claim
2 1, wherein the thickness of the passivation structure is
3 between 3 and 4 μ m.

1 8. The interconnect structure as claimed in claim
2 1, wherein the opening in the passivation structure is
3 rectangular.

1 9. A method for fabricating an interconnect
2 structure on a TFT-array substrate of a flat panel
3 display, comprising:

4 forming a plurality of first metal lines in a non-
5 display area of the TFT-array substrate;

6 forming a first insulating layer on the TFT-array
7 substrate to cover the first metal lines;

8 forming a plurality of second metal lines on the
9 first insulating layer, wherein each second

10 metal line corresponds with one first metal
11 line;
12 forming a second insulating layer covering the
13 second metal lines and the first insulating
14 layer;
15 forming a passivation structure on the second
16 insulating layer with openings therein to
17 expose one end of every first and its
18 corresponding second metal lines;
19 forming a plurality of first and second via holes in
20 the first and second insulating layers inside
21 the opening of the passivation structure to
22 expose the first and second metal lines
23 respectively;
24 forming an ITO (indium tin oxide) layer on the
25 second insulating layer, filling the first and
26 second via holes to connect the first and
27 second metal lines;
28 forming a patterned photoresist layer on the ITO
29 layer, masking the ITO layer inside the opening
30 of the passivation structure;
31 etching the ITO layer with the patterned photoresist
32 layer as a mask to form ITO wiring to connect
33 the first metal line with the second metal
34 line; and
35 removal of the remaining photoresist layer.

1 10. The method as claimed in claim 9, wherein the
2 first metal line is formed simultaneously with gate metal

3 lines formed in a display area of the TFT-array
4 substrate.

1 11. The method as claimed in claim 9, wherein the
2 second metal line is formed simultaneously with
3 source/drain metal lines formed in a display area of the
4 TFT-array substrate.

1 12. The method as claimed in claim 9, wherein the
2 thickness of the passivation structures is between 3 and
3 4 μ m.

1 13. The method as claimed in claim 9, wherein the
2 opening of the passivation structure is rectangular.